ABSTRACT OF THE DISCLOSURE

A memory unit and memory module using the same. The memory module at least has a first memory region with a plurality of memory units. In each memory unit, first and access transistors each have a first terminal coupled to one bit line pair respectively. A latch node is coupled between second terminals of the first and second access transistor to latch data. An OR gate has a first input terminal coupled to a word line, an output terminal coupled to gates of the first and second access transistor, and a second input terminal. The second input terminals of the OR gates in all memory units are coupled to a flush line. Invalidation information is written to the latch nodes in the memory units from the bit line pair when the flush line is activated during a flush operation.